



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,855	06/08/2001	Kinya Osa	862.C2255	9364
5514	7590	10/31/2005	EXAMINER	
FITZPATRICK CELLA HARPER & SCINTO			LAROSE, COLIN M	
30 ROCKEFELLER PLAZA			ART UNIT	
NEW YORK, NY 10112			PAPER NUMBER	

2627

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/875,855

Applicant(s)

OSA, KINYA

Examiner

Colin M. LaRose

Art Unit

2623

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 August 2005 has been entered.

Response to Amendments and Arguments

2. Applicant's remarks with respect to claim 1 have been considered but are not persuasive for the following reasons. Applicant argues that the combination of Yip EU and Yip AU is improper because, in Yip AU, "bit-plane coding ... must be executed for all bit-planes, and the number of bit-planes to be coded can not be reduced" (see Remarks, p. 11). In other words, Applicant seems to assert that since Yip AU allegedly discloses transforming and analyzing all of the bit planes for bit-plane coding, rather than only the significant bit planes, that the combination of Yip EU and Yip AU "would not attain the effects of claim 1 in which the number of bit-planes to be coded can be reduced" (Remarks, p. 11).

Examiner respectfully disagrees with these assertions. Yip AU teaches building a bit-plane tree and detecting the significant bit planes from the tree. Then, during the bit-plane coding performed by the bit-plane encoder 610, it appears that only significant bit-planes are encoded (see pp. 19-20, which describes how the bit plane encoder parses the significant from the insignificant nodes in the tree – the insignificant nodes and their children are zeroed out before

Art Unit: 2623

being placed into lists so that they are not subsequently encoded). Thus, Yip AU can be considered to teach encoding only the significant bit-planes, as required by the claim.

The claim calls for the insignificant bits to be “omitted from coding,” however, there are no restrictions placed on which bits are *sent* to the bit-plane processor for coding. The claim therefore embraces a system that detects the significant bits, transfers all of the significant bits (and optionally insignificant bits as well) to the bit-plane processor, and then codes only the significant bits with the bit-plane processor. Yip AU is considered to disclose such a process.

Nevertheless, Yip AU was only relied upon to show that it was conventional and obvious to transfer a data group between two memories and to detect the MSBs, or maximum values, of the data group while transferring the data between the memories. Omitting the insignificant bits from coding (i.e. the bits “in a higher position than the highest-order bit position specified”) is well taught by Yip EU, and whether Yip AU discloses such a feature is essentially immaterial to the proposed combination. The proposed modification of Yip EU to include Yip AU’s two memories in order to facilitate the transfer of a data group and auxiliary information pertaining to the significant/insignificant bits of the data group, and to detect such auxiliary information while transferring the data group, would not be negated by Yip AU failing to omit the insignificant bits from coding.

Regarding claim 2, Applicant asserts that Yip EU does not disclose “performing a logical OR calculation independently for each bit-plane,” as claimed. Applicant uses Yip EU’s calculation, $B = B' + (\text{BitB1} + \text{BitB2} + \text{BitB3})$, to illustrate that Yip EU’s logical OR calculation is not independent for each bit-plane. In the above example, Applicant points out that B' depends

Art Unit: 2623

on previous bit-plane calculations and reasons that Yip EU therefore does not “perform a logical OR calculation independently for each bit-plane.” However, Examiner respectfully points out that the “(BitB1 + BitB2 + BitB3)” calculation is considered “a logical OR calculation” that is “independent” for each bit-plane. The (BitB1 + BitB2 + BitB3) is ORed with the B’ value, which is dependent on other bit-planes, but this does not negative the fact that a logical OR calculation, such as (BitB1 + BitB2 + BitB3), is independently performed for each bit plane.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over European Patent Application 0905978 A2 by Yip et al. (“Yip EU”) in view of Australian Patent Publication 199957151 A1 by Yip et al. (“Yip AU”).

Regarding claims 1 and 8, Yip EU discloses a circuit and method (figure 3) for transferring a data group (i.e. coefficients of image data) having data represented by plural bits to a bit-plane coding processor (i.e. coding routine 314), comprising:

detection means for detecting a maximum value in the data group as a transfer object (306 and ¶ 32: the largest coefficient in the data group is identified); and

Art Unit: 2623

specifying means for specifying a non-zero highest-order bit position among bits constructing the maximum value detected by said detection means (306 and ¶ 32: the MSB bit position (i.e. the highest significant bitplane) of the maximum detected value is specified as “maxBitNumber”), and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor (figure 3: “maxBitNumber” is output to the coder 314),

wherein a bit in a position higher than the highest-order bit position specified by said specifying means is omitted from coding executed by said bit-plane coding processor (Figure 4 shows the “Code region” routine of figure 3. As can be seen in figure 4, coding begins with the “maxBitNumber” bitplane and continues until the “minBitNumber” bitplane is reached. As a result, those bits in the bitplanes higher than the “maxBitNumber” bitplane are omitted from processing.)

Yip EU does not appear to disclose transferring “from a first memory to a second memory for coding... after transferring the data group to the second memory.” Cf. figure 1 of Yip EU, which shows coding (120) an image that has been transformed (110) but does not show transfer of the coefficients to or from memory.

Yip EU also does not disclose detecting “while transferring the data group and completed before completion of the transfer.” Cf. figure 1 of Yip EU, which shows that coefficients are transferred to the coding block (120), where the detecting (306) and coding (314) occur, but there is no transfer between memories shown.

Yip AU discloses a bit-plane encoding system (figure 6) that is very similar to that of Yip EU. In particular, Yip AU discloses receiving coefficients into a first memory (612), and then converting the coefficients into bitplanes (606) and building a tree (608-0 – 608-15), which detects significant bitplanes in a quadtree fashion (see figure 7). The bitplane and tree information are then stored in a second memory (614,616, and 619-0 – 618-15) for output to the encoder (610). While the data is being transferred from the first memory (612) to the second memory (614,616, and 619-0 – 618-15), the bitplane analysis (606 and 608-0 – 608-15) is executed.

Thus, Yip AU teaches receiving wavelet coefficients in a memory (612), performing a bit-plane analysis on the coefficients (606 and 608-0 – 608-15), storing the results of the analysis in memory (614,616, and 619-0 – 618-15), and then outputting the results to a bit-plane encoder (610). This process is similar to that of Yip EU, wherein wavelet coefficients are transferred to a processor (120) where bit-plane analysis is performed (306), and the coefficients are then encoded on the basis of the results of the analysis (314). The primary difference is that Yip AU includes two memories for facilitating the transfer of data to the encoder.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yip EU by Yip AU to achieve the claimed invention by transferring the data group from a first memory to a second memory and detecting a maximum value in the data group while transferring the data group, as claimed, since Yip AU teaches that when wavelet-transformed image data is to be encoded on the basis of significant bit planes, it was advantageous and conventional to include two memories, as claimed, in order to facilitate the transfer of data to the encoder. In addition, Yip AU shows that it was conventional to perform a bitplane analysis to

Art Unit: 2623

detect significant bitplanes while transferring the data from the first to the second memory (see figure 6).

Regarding claims 6 and 12, Yip EU discloses including any known memory circuit, which includes a DMA circuit (§ 142).

Regarding claim 7, Yip EU discloses the data group includes transform coefficients generated by transform coding on the pixel data (304, figure 3).

Regarding claims 2 and 9, Yip EU discloses a circuit and method (figure 3) for transferring a data group (i.e. coefficients of image data) having data represented by plural bits to a bitplane coding processor (i.e. coding routine 314), comprising:

calculation means for performing logical OR calculation independently for each bit-plane, each bit plane comprising bits which are located at a same bit position among bits constructing data which all the data group has (306 and ¶ 32: the largest coefficient in the data group is identified; figure 29, and ¶ 123: the “bit-plane unit” in figure 29 performs an independent logical OR operation on bits in a current bit plane (e.g. “BitB1 + BitB2 + BitB3” on p. 15) in order to generate “data valid bits,”); and

specifying means for specifying a non-zero highest-order bit position among bits constructing a result of the logical OR calculation by said calculation means (306 and ¶ 32: the MSB bit position (i.e. the highest significant bitplane) of the maximum detected value is specified as “maxBitNumber”; and ¶ 126: the data valid bits are used for determining the most significant data bit) and outputting a code representing the bit position specified by said

Art Unit: 2623

specifying means to said bit-plane coding processor (figure 3: “maxBitNumber” is output to the coder 314),

wherein a bit in a position higher than said highest-order bit position specified by said specifying means is omitted from coding executed by said bitplane coding processor (Figure 4 shows the “Code region” routine of figure 3. As can be seen in figure 4, coding begins with the “maxBitNumber” bitplane and continues until the “minBitNumber” bitplane is reached. As a result, those bits in the bitplanes higher than the “maxBitNumber” bitplane are omitted from processing.).

Yip EU is deficient for claims 2 and 9 for the same reasons as recited above for claims 1 and 8; and Yip AU is relied upon to cure the deficiencies of Yip EU for claims 2 and 9. Please refer to the explanation of the combination for claims 1 and 8 above.

Regarding claims 3 and 10, Yip EU discloses a circuit and method (figure 3) for transferring a data group (i.e. bitplanes of coefficients) having data represented by plural bits from coding by a bitplane coding processor (i.e. coding routine 314), comprising:

calculation means for performing logical OR calculation independently for each bit-plane, each bit plane comprising bits which are located at a same bit position among bits constructing data which all the data group has (figure 29, and ¶ 123: the “bit-plane unit” in figure 29 performs an independent logical OR operation on bits in a current bit plane (e.g. “BitB1 + BitB2 + BitB3” on p. 15) in order to generate “data valid bits,”); and

specifying means for specifying a non-zero lowest-order bit position among bits constructing the result of the logical OR calculation by said calculation means (see ¶ 33: a non-

Art Unit: 2623

zero lowest-order bit position, corresponding to the “minBitNumber” bitplane, is designated according to the desired image quality; and Yip’s lowest-order bit position is “among bits constructing the result of the logical OR calculation” – since all bits in bitplanes lower than the maxBitNumber bitplane are used to construct the results of the logical OR calculation in ¶ 123, the designated lowest-order bitplane (“minBitNumber”) comprises bits used to construct the results of the logical OR calculation) and outputting a code representing the bit position specified by said specifying means to said bit-plane coding processor (figure 3: “maxBitNumber” is output to the coder 314),

wherein a bit in a position lower than said lowest-order bit position specified by said specifying means is omitted from coding by said bitplane coding processor (Figure 4 shows the “Code region” routine of figure 3. As can be seen in figure 4, coding begins with the “maxBitNumber” bitplane and continues until the “minBitNumber” bitplane is reached. As a result, those bits in the bitplanes lower than the “minBitNumber” plane are omitted from processing.).

Yip EU is deficient for claims 3 and 10 for the same reasons as recited above for claims 1 and 8; and Yip AU is relied upon to cure the deficiencies of Yip EU for claims 3 and 10. Please refer to the explanation of the combination for claims 1 and 8 above.

Regarding claims 4 and 11, it is noted that claim 4 is a combination of claims 2 and 3, and claim 11 is a combination of claims 9 and 10, the corresponding features of claims 2, 3, 9, and 10 being disclosed by Yip EU as recited above.

Art Unit: 2623


Yip EU is deficient for claims 4 and 11 for the same reasons as recited above for claims 1 and 8; and Yip AU is relied upon to cure the deficiencies of Yip EU for claims 4 and 11. Please refer to the explanation of the combination for claims 1 and 8 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (571) 272-7423. If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Bhavesh Mehta, can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CML
Group Art Unit 2627
21 October 2005


VIKKRAM BALI
PRIMARY EXAMINER